CLAIM AMENDMENTS

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) A maximum likelihood bit synchronizer for use in a communication system including a transmitter that generates a transmitter signal at a first rate and a receiver that samples the transmitter signal at ~~a higher rate~~ a second rate higher than the first rate and generates a receiver signal, said synchronizer comprising:

a tapped delay line;

n timing hypothesis circuits coupled to said tapped delay line, wherein n is an integer equal to ~~the sampling rate divided by said first rate~~ the second rate divided by the first rate plus two, wherein each of said n timing hypothesis circuits includes a sum-and-dump summer connected to n-2 outputs of said tapped delay line; and

a control and adjudication circuit coupled to said n timing hypothesis circuits that compares outputs of said n timing hypothesis circuits and selects one of said n timing hypothesis circuits.

2. (Original) The synchronizer of claim 1 further comprising an antipodal circuit coupled to an input of said tapped delay line for generating an antipodal signal from said receiver signal.

3. (Original) The synchronizer of claim 2 wherein said antipodal circuit includes an average level estimator.

4. (Currently Amended) The synchronizer of claim 3 wherein said antipodal circuit further includes a summing circuit that receives ~~said antipodal~~ a level estimator signal and said receiver signal and ~~that~~ generates said antipodal signal.

5. (Original) The synchronizer of claim 1 wherein the receiver signal is a general bilevel signal independent of modulation type.

6. (Original) The synchronizer of claim 1 wherein the transmitter signal is selected from the group consisting of on-off keyed signals and FSK signals.

7. (Original) The synchronizer of claim 1 wherein said tapped delay line includes n plus 2 delay elements.

8. Cancelled.

9. (Currently Amended) The synchronizer of claim [[8]] 1 wherein each of said n timing hypothesis circuits further includes an absolute value circuit that is connected to said sum-and-dump summer.

10. (Currently Amended) The synchronizer of claim 9 wherein each of

said n timing hypothesis circuits further includes an averaging circuit coupled to said absolute value circuit.

11. (Original) The synchronizer of claim 10 wherein said averaging circuit is a sliding window summer.

12. (Currently Amended) The synchronizer of claim [[11]] 10 wherein said averaging circuit ~~is~~ includes a single pole, unity gain, low-pass filter.

13. (Currently Amended) The synchronizer of claim [[8]] 1 further comprising a select switch coupled to said sum-and-dump summers, wherein said select switch receives a switch control signal from said control and adjudication ~~circuits~~ circuit that selects an output signal of one of said sum-and-dump summers.

14. (Original) The synchronizer of claim 13 further comprising a threshold test circuit that compares said selected output signal to a threshold value and outputs one of a mark symbol or a space symbol.

15. (Currently Amended) The synchronizer of claim 14 further comprising an output control circuit that receives an output control signal from said control and adjudication circuit, wherein said output control circuit outputs zero, one, ~~or~~ two mark symbols or two space signals in response to said output control signal.

16. (Currently Amended) A maximum likelihood bit synchronizer coupled to a receiver that generates a receiver signal, comprising:

an average level estimator coupled to said receiver signal that generates an average signal;

a summing circuit coupled to said receiver signal and said average signal ~~and~~ that outputs an antipodal signal;

a tapped delay line coupled to said summing circuit;

a plurality of timing hypothesis circuits coupled to said tapped delay line, wherein each of said timing hypothesis circuits include a data detector, an absolute value circuit connected to said data detector, and an averaging circuit connected to said absolute value circuit; and

a control and adjudication circuit coupled to said timing hypothesis circuits that compares outputs of said timing hypothesis circuits and selects one of said timing hypothesis circuits.

17. (Currently Amended) The maximum likelihood bit synchronizer of claim 16 wherein n timing hypothesis circuits are provided and wherein n is the greatest integer that is equal to ~~a symbol rate divided by a sampling rate~~ a transmitter rate divided by a sampling rate of the received signal plus 2.

18. (Original) The maximum likelihood bit synchronizer of claim 16 further comprising a select switch connected to said data detectors of said timing hypothesis circuits and to said control and adjudication circuit.

19. (Currently Amended) The maximum likelihood bit synchronizer of claim 18 further comprising:

a threshold test circuit that compares ~~said~~ a selected signal from the selector switch to a threshold value and outputs one of a mark symbol and a space symbol; and

an output control circuit that outputs zero, one, ~~or~~ two mark symbols or two space symbols.

20. (Original) The maximum likelihood bit synchronizer of claim 16 wherein the receiver signal is a general bilevel signal independent of modulation type.

21. (Original) The maximum likelihood bit synchronizer of claim 16 wherein said receiver signal is selected from the group consisting of on-off keyed signals and FSK signals.

22. (Currently Amended) The maximum likelihood bit synchronizer of claim [[16]] 17wherein said tapped delay line includes ~~(n+2)~~ n+2 delay elements.

23. (Currently Amended) The maximum likelihood bit synchronizer of claim [[16]] 17 wherein said data detector is a sum-and-dump summer connected to ~~(n-2)~~ n-2 outputs of said tapped delay line.

24. (Original) The maximum likelihood bit synchronizer of claim 16 wherein said averaging circuit is a sliding window summer.

25. (Currently Amended) The maximum likelihood bit synchronizer of claim 16 wherein said averaging circuit ~~is~~ includes a single pole, unity gain, low-pass filter.

26. (Currently Amended) The maximum likelihood bit synchronizer of claim [[18]] 19 wherein said control and adjudication circuit outputs a switch control signal to said select switch to select an output of one of said data detectors and an output control signal to said output control circuit to select output of zero, one, ~~or~~ two mark symbols or two space symbols.

27. (New) A maximum likelihood bit synchronizer for use in a communications system including a transmitter that generates a transmitter signal at a first rate and a receiver that samples the transmitter signal at a second rate higher than the first rate and generates a receiver signal, said synchronizer comprising:

a tapped delay line;

n timing hypothesis circuits coupled to said tapped delay line, wherein n is an integer equal to the second rate divided by the first rate plus two;

an antipodal circuit coupled to an input of the tapped delay line for generating an antipodal signal from the receiver signal, said antipodal circuit

including an average level estimator; and

a control and adjudication circuit coupled to said n timing hypothesis circuits that compares outputs of said n timing hypothesis circuits and selects one of said n timing hypothesis circuits.

28. (New) The synchronizer of claim 27 wherein said antipodal circuit further includes a summing circuit that receives a level estimator signal and said receiver signal generates said antipodal signal.

29. (New) The synchronizer of claim 27 wherein the receiver signal is a general bilevel signal independent of modulation type.

30. (New) The synchronizer of claim 27 wherein the transmitter signal is selected from the group consisting of on-off keyed signals and FSK signals.

31. (New) The synchronizer of claim 27 wherein said tapped delay line includes n plus 2 delay elements.

32. (New) The synchronizer of claim 27 wherein each of said n timing hypothesis circuits includes a sum-and-dump summer connected to n-2 outputs of said tapped delay line.

33. (New) The synchronizer of claim 32 wherein each of said n

timing hypothesis circuits further includes an absolute value circuit that is connected to said sum-and-dump summer.

34. (New) The synchronizer of claim 33 wherein each of said n timing hypothesis circuits further includes an averaging circuit coupled to said absolute value circuit.

35. (New) The synchronizer of claim 34 wherein said averaging circuit is a sliding window summer.

36. (New) The synchronizer of claim 34 wherein said averaging circuit includes a single pole, unity gain, low-pass filter.

37. (New) The synchronizer of claim 32 further comprising a select switch coupled to said sum-and-dump summers, wherein said select switch receives a switch control signal from said control and adjudication circuit that selects an output signal of one of said sum-and-dump summers.

38. (New) The synchronizer of claim 37 further comprising a threshold test circuit that compares said selected output signal to a threshold value and outputs one of a mark symbol or a space symbol.

39. (New) The synchronizer of claim 38 further comprising an output

control circuit that receives an output control signal from said control and adjudication circuit, wherein said output control circuit outputs zero, one, two mark symbols or two space signals in response to said output control signal.